Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BAL 2**
2. **IN –**
3. **IN +**
4. **V –**
5. **NC**
6. **BC**
7. **OUT**
8. **V +**
9. **BAL 1**

**9 8 7 6**

**1 2 3 4**

**5**

**MASK**

**REF**

**50389A1**

**.072”**

**103”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V -**

**Mask Ref: 50389A1**

**APPROVED BY: DK DIE SIZE .072” X .103” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HA0-5177-6**

**DG 10.1.2**

#### Rev B, 7/19/02